IN THE CLAIMS:

Cancel: 1-112, without prejudice.

Add new claims as follows:

1-112. (Canceled)

113. (New) A multi-mode PAM output driver for driving a symbol, the output driver comprising:

logic circuitry; and

a driver circuit coupled to the logic circuitry and configured to drive the symbol;

wherein the multi-mode PAM output driver is capable of operating in a specified mode of a plurality of predefined modes;

wherein the symbol is an N-PAM symbol when the specified mode is a first mode;

wherein the symbol is an M-PAM symbol when the specified mode is a second mode; and

wherein N is not equal to M.

114. (New) The multi-mode PAM output driver of claim 113, wherein N is equal to 2.

115. (New) The multi-mode PAM output driver of claim 113, wherein N is equal to 2 and M is equal to 4.

116. (New) The multi-mode PAM output driver of claim 113, wherein M and N are both integers selected from the group consisting of 2, 4, 8, and 16.

117. (New) The multi-mode PAM output driver of claim 113, wherein the output driver drives the symbol onto a multi-drop bus.

118. (New) The multi-mode PAM output driver of claim 113,

wherein the logic circuitry is configured to receive data;

wherein, when the specified mode is a first mode, the driver circuit outputs signals representing the received data, the signals including one or more N-PAM modulated symbols; and

wherein, when the specified mode is a second mode, the driver circuit outputs signals representing the received data, the signals including one or more M-PAM modulated symbols.

119. (New) The multi-mode PAM output driver of claim 118, wherein, when the specified mode is a second mode, the received data comprises at least two bits including a most significant bit (MSB) and a least significant bit (LSB).

120. (New) The multi-mode PAM output driver of claim 118, wherein the received data represents at least part of an address in a memory system.

121. (New) The multi-mode PAM output driver of claim 118, wherein the received data represents at least part of a value stored in a memory system.

122. (New) The multi-mode PAM output driver of claim 118, wherein the received data represents at least part of a command in a memory system.

123. (New) The multi-mode PAM output driver of claim 113,

wherein, when the specified mode is a first mode, the driver circuit drives a sequence of symbols representing received data at a first symbol rate, the sequence of symbols including one or more N-PAM modulated symbols;

wherein, when the specified mode is a second mode, the driver circuit drives a sequence of symbols representing the received data at a second symbol rate, the sequence of symbols including one or more M-PAM modulated symbols; and

wherein the first symbol rate is not equal to the second symbol rate.

124. (New) The multi-mode PAM output driver of claim 123, wherein the first symbol rate is twice the second symbol rate.

125. (New) The multi-mode PAM output driver of claim 123, wherein the ratio between the second symbol rate and the first symbol rate is equal to $\log_2(N)/\log_2(M)$.

126. (New) A multi-mode PAM receiver for receiving a symbol, the receiver comprising:

a receiver circuit configured to receive the symbol; and

logic circuitry coupled to the receiver circuit;

wherein the multi-mode PAM receiver is capable of operating in a specified mode of a plurality of predefined modes;

wherein the received symbol is an N-PAM symbol when the specified mode is a first mode;

wherein the received symbol is an M-PAM symbol when the specified mode is a second mode; and

wherein N is not equal to M.

127. (New) The multi-mode PAM receiver of claim 126, wherein N is equal to 2.

128. (New) The multi-mode PAM receiver of claim 126, wherein N is equal to 2 and M is equal to 4.

129. (New) The multi-mode PAM receiver of claim 126, wherein M and N are both integers selected from the group consisting of 2, 4, 8, and 16.

130. (New) The multi-mode PAM receiver of claim 126, wherein the receiver circuit outputs one or more binary signals.

131. (New) The multi-mode PAM receiver of claim 130, where the receiver circuit outputs the one or more binary signals synchronized to a clock signal.

132. (New) The multi-mode PAM receiver of claim 126, wherein the receiver circuit latches the symbol at a symbol rate selected from a plurality of predefined symbol rates.

133. (New) The multi-mode PAM receiver of claim 126, wherein, when the specified mode is a second mode, the received symbol represents two or more bits including a most significant bit (MSB) and a least significant bit (LSB).

134. (New) The multi-mode PAM receiver of claim 126, wherein the received symbol represents at least a part of an address in a memory system.

135. (New) The multi-mode PAM receiver of claim 126, wherein the received symbol represents at least a part of a value stored in a memory system.

136. (New) The multi-mode PAM receiver of claim 126, wherein the received symbol represents at least a part of a command in a memory system.

137. (New) The multi-mode PAM receiver of claim 126,

wherein, when the specified mode is a first mode, the receiver circuit receives a sequence of symbols at a first symbol rate, the sequence of symbols including one or more N-PAM modulated symbols;

wherein, when the specified mode is a second mode, the receiver circuit receives a sequence of symbols at a second symbol rate, the sequence of symbols including one or more M-PAM modulated symbols; and

wherein the first symbol rate is not equal to the second symbol rate.

138. (New) The multi-mode PAM receiver of claim 137, wherein the first symbol rate is twice the second symbol rate.

139. (New) The multi-mode PAM receiver of claim 137, wherein the ratio between the second symbol rate and the first symbol rate is equal to $\log_2(N)/\log_2(M)$.

140. (New) The multi-mode PAM receiver of claim 126,

wherein the receiver circuit comprises a first receiver circuit and a second receiver circuit, each of the first and the second receiver circuits configured to output one or more signals;

wherein the signals output by the first receiver circuit represent a most significant bit (MSB) of the symbol; and

wherein, when the specified mode is a second mode, the signals output by the second receiver circuit represent a least significant bit (LSB) of the symbol.

141. (New) The multi-mode PAM receiver of claim 140,

wherein the first receiver circuit includes a MSB latching comparator to compare the symbol to a first reference voltage to generate a first signal representing a state of the MSB;

wherein the second receiver circuit includes a first LSB latching comparator to compare the input symbol to a second reference voltage and to generate a second signal representing a relationship between the symbol and the second reference voltage;

wherein the second receiver circuit includes a second LSB latching comparator to compare the input symbol to a third reference voltage and to generate a third signal representing a relationship between the symbol and the third reference voltage; and

wherein the second receiver circuit includes logic circuitry configured to generate a fourth signal representing a state of the LSB based, at least in part, on the second signal and the third signal.

142. (New) A multi-mode PAM transceiver comprising:

a multi-mode PAM output driver, configured to output a first stream of signals at a symbol rate on a first signal path; and

a multi-mode PAM receiver, configured to receive a second stream of signals at the symbol rate from a second signal path;

wherein the first stream of signals includes an N-PAM modulated symbol when a mode signal is in a first mode signal state;

wherein the first stream of signals includes an M-PAM modulated symbol when the mode signal is in a second mode signal state; and

where N is not equal to M.

143. (New) The multi-mode PAM transceiver of claim 142, wherein the multi-mode PAM output driver and multi-mode PAM receiver are embodied on a single integrated circuit.

144. (New) The multi-mode PAM transceiver of claim 142, wherein the first signal path and second signal path comprise the same physical medium.

145. (New) The multi-mode PAM transceiver of claim 144, wherein the signal path is a multi-drop bus.

146. (New) The multi-mode PAM transceiver of claim 142, wherein the first stream of signals includes at least one symbol representing at least a part of an address in a memory system.

147. (New) The multi-mode PAM transceiver of claim 142, wherein the first stream of signals includes at least one symbol representing at least a part of a value stored in a memory system.

148. (New) The multi-mode PAM transceiver of claim 142, wherein the first stream of signals includes at least one symbol representing at least a part of a command in a memory system.

149. (New) The multi-mode PAM transceiver of claim 142, wherein N is equal to two.

150. (New) The multi-mode PAM transceiver of claim 142, wherein N is equal to two and M is equal to four.

151. (New) The multi-mode PAM transceiver of claim 142, wherein M and N are both integers selected from the group consisting of 2, 4, 8, and 16.

152. (New) The multi-mode PAM transceiver of claim 142, wherein the state of the mode signal is determined by a hardware setting.

153. (New) The multi-mode PAM transceiver of claim 142, wherein the symbol rate is determined by control logic, and the control logic determines the state of the mode signal based, at least in part, on the second stream of signals.

154. (New) The multi-mode PAM transceiver of claim 142, wherein the symbol rate is selected from amongst a plurality of distinct symbol rates.

155. (New) The multi-mode PAM transceiver of claim 142, wherein the symbol rate is determined by selecting the symbol rate from amongst a plurality of symbol rates, the plurality of symbol rates including a first symbol rate and a second symbol rate, wherein the second symbol rate is twice the first symbol rate.

156. (New) The multi-mode PAM transceiver of claim 142, wherein the symbol rate is determined by selecting the symbol rate from amongst a plurality of symbol rates, the plurality of symbol rates including a first symbol rate and a second symbol rate, wherein the ratio between the second symbol rate and the first symbol rate is equal to $\log_2(N)/\log_2(M)$.

157. (New) The multi-mode PAM transceiver of claim 142,

wherein, when a mode signal is in a first mode signal state, the first stream of signals output by the output driver is output at a first symbol rate, the first stream of signals including one or more N-PAM modulated symbols;

wherein, when a mode signal is in a second mode signal state, the second stream of signals output by the output driver is output at a second symbol rate, the second stream of signals including one or more M-PAM modulated symbols; and

wherein the first symbol rate is not equal to the second symbol rate.

158. (New) The multi-mode PAM transceiver of claim 157, wherein the first symbol rate is twice the second symbol rate.

159. (New) The multi-mode PAM transceiver of claim 157, wherein the ratio between the second symbol rate and the first symbol rate is equal to $\log_2(N)/\log_2(M)$.

160. (New) The multi-mode PAM transceiver of claim 142,

wherein the first stream of signals has an associated first data rate when a mode signal is in a first mode signal state;

wherein the second stream of signals has an associated second data rate when the mode signal is in a second mode signal state; and

wherein the symbol rate is selected so as to make the first data rate equal to the second data rate.

161. (New) A method of data transmission, comprising:

configuring an multi-mode PAM output driver to operate in a specified mode of a plurality of predefined modes;

receiving data at the multi-mode PAM output driver;

using the multi-mode PAM output driver, outputting a symbol corresponding to at least a portion of the received data;

wherein the symbol is an N-PAM symbol when a specified mode is a first mode;

wherein the symbol is an M-PAM symbol when the specified mode is a second mode; and

wherein N is not equal to M.

162. (New) The method of claim 161, wherein M and N are both integers selected from the group consisting of 2, 4, 8, and 16.

163. (New) The method of claim 161, the method further including:

operating the multi-mode PAM output driver so as to drive a sequence of symbols onto a first signal path at a predetermined symbol rate, the sequence comprising a plurality of symbols, each symbol having a respective level of a predetermined number of PAM levels;

receiving, at a multi-mode PAM receiver, the sequence of symbols from a second signal path;

determining, based on a relationship between the sequence of driven symbols and the sequence of received symbols, an error metric; and

when the error metric is greater than an error metric threshold,

decreasing the symbol rate, the number of PAM levels, or both, and

subsequently repeating the operating the multi-mode PAM output driver, receiving at the multi-mode PAM receiver, and determining the error metric.

164. (New) The method of claim 163, wherein the multi-mode PAM output driver and multi-mode PAM receiver are embodied on a single integrated circuit.

165. (New) The method of claim 163, wherein the first signal path and second signal path comprise the same physical medium.

166. (New) The method of claim 165, wherein the signal path is a multi-drop bus.

167. (New) The method of claim 163, wherein the operating the multi-mode PAM output driver, receiving at the multi-mode PAM receiver, and determining the error metric are performed periodically at a rate defined by a predetermined interval of time.

168. (New) The method of claim 163, wherein the symbol rate is initially one of a plurality of available symbol rates and the number of PAM levels is initially one of a plurality of available numbers of PAM levels, the method further comprising:

when the error metric is less than or equal to the error metric threshold and either

the symbol rate is not the maximum symbol rate in the plurality of symbol rates, or

the number of PAM levels is not the maximum number of PAM levels in the plurality of numbers of PAM levels,

increasing the symbol rate, the number of PAM levels, or both, and

subsequently repeating the operating the multi-mode PAM output driver, receiving at the multi-mode PAM receiver, and determining the error metric.

169. (New) The method of claim 168, wherein the symbol rate is determined by selecting the symbol rate from amongst the plurality of available symbol rates, the plurality of available rates including a first symbol rate and a second symbol rate, wherein the second symbol rate is twice the first symbol rate.

170. (New) The method of claim 168, wherein the symbol rate is determined by selecting the symbol rate from amongst the plurality of available symbol rates, the plurality of available rates including a first symbol rate and a second symbol rate, wherein the ratio between the second symbol rate and the first symbol rate is equal to $\log_2(N)/\log_2(M)$.

171. (New) The method of claim 161, the method further including;

operating the multi-mode PAM output driver so as to drive a first sequence of symbols at a first symbol rate selected from a plurality of predetermined symbol rates, the

sequence comprising a plurality of symbols, each symbol having a respective level of a first number of PAM levels, the first number of PAM levels selected from a plurality of available PAM levels;

receiving at a multi-mode PAM receiver the first sequence of symbols;

determining, based on voltage and timing characteristics of the first sequence of received symbols, a first set of signal characteristics, the set of signal characteristics corresponding to the first symbol rate and to the first number of PAM levels;

operating the multi-mode PAM driver so as to drive a second sequence of symbols at a second symbol rate selected from the plurality of predetermined symbol rates, the sequence comprising a plurality of symbols, each symbol having a respective level of a second number of PAM levels, the second number of PAM levels selected from the plurality of available PAM levels;

receiving at a multi-mode PAM receiver the second sequence of symbols;

determining, based on voltage and timing characteristics of the second sequence of received symbols, a second set of signal characteristics, the set corresponding to the second symbol rate and to the second level of predetermined number of PAM levels;

based on the first and the second set of characteristics, choosing a mode of operation of the system, the mode of operation specified, at least, by a symbol rate and a number of PAM levels.

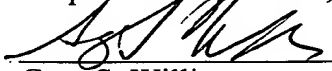
## CONCLUSION

The pending claims are now properly numbered 113-171.

The Examiner is invited to call the undersigned attorney at (650) 493-4935 if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 25, 2003



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